EGC442
Class Notes
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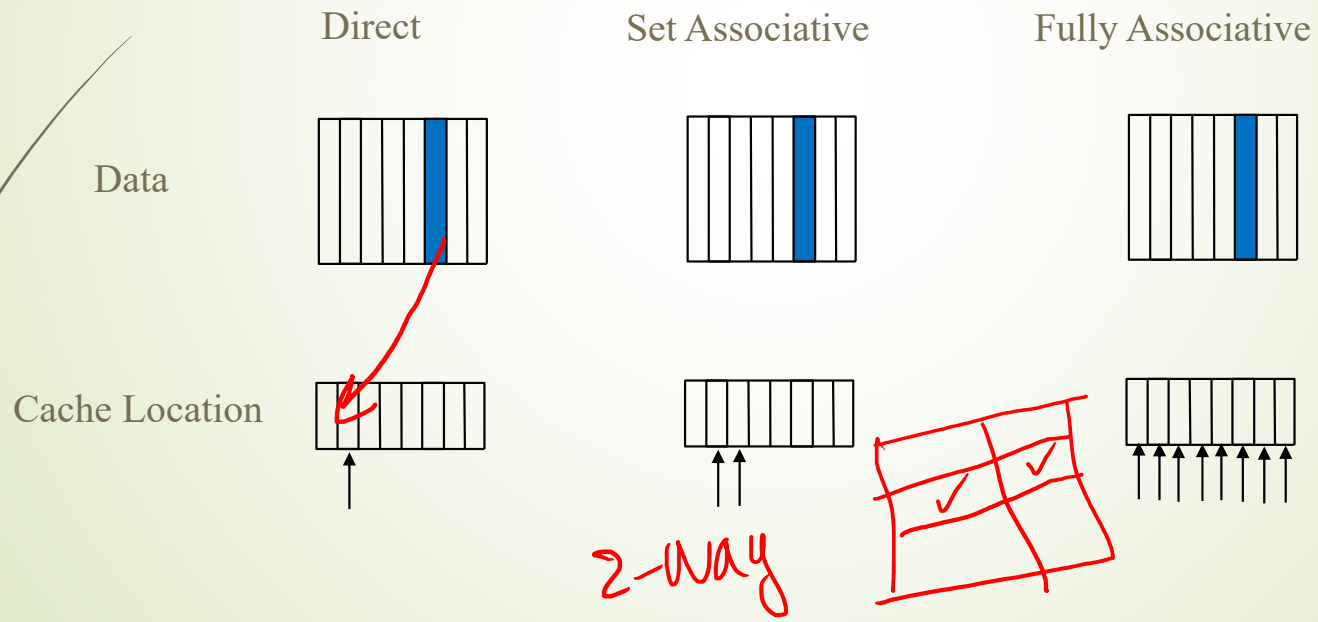
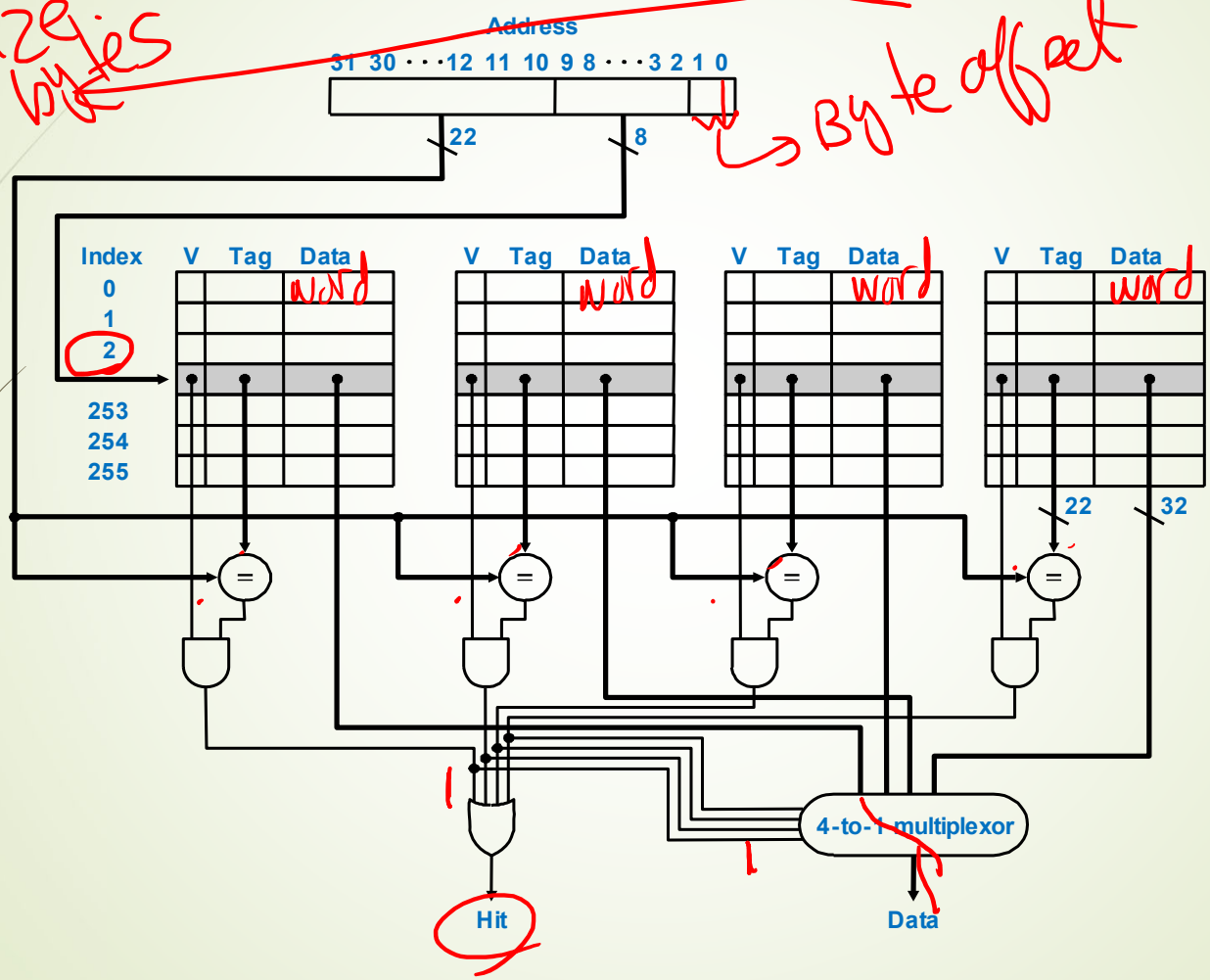
Decreasing Miss Ratio with Associativity

Associativity: Reducing cache misses by more flexible placement of blocks

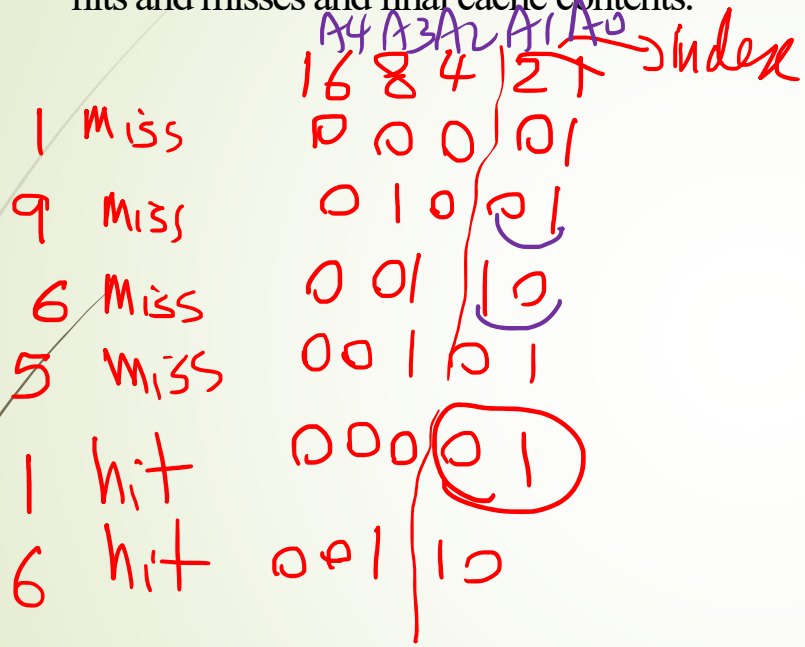


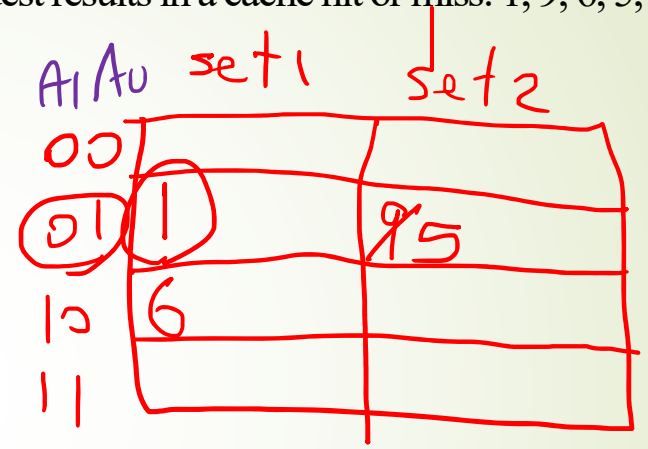
4-Way Associative Cache Organization



random replacement

1) Assume a two-way set-associative cache with one byte word size, 8-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 1, 6. Show the hits and misses and final cache contents.



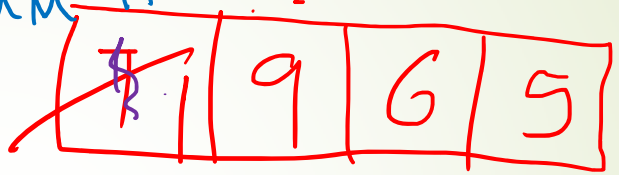


FIFO

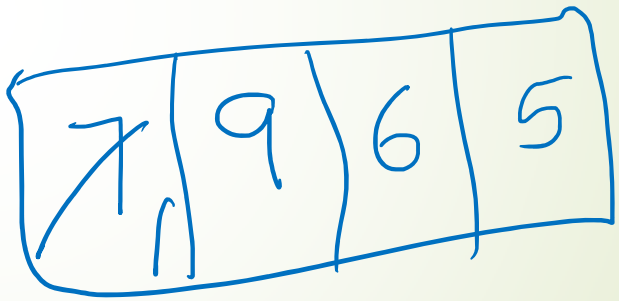
word size = 1 byte

2) Assume a fully associative cache with 4-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 7, 9, 6, 5, 1, 6. Show the hits and misses and final cache contents.

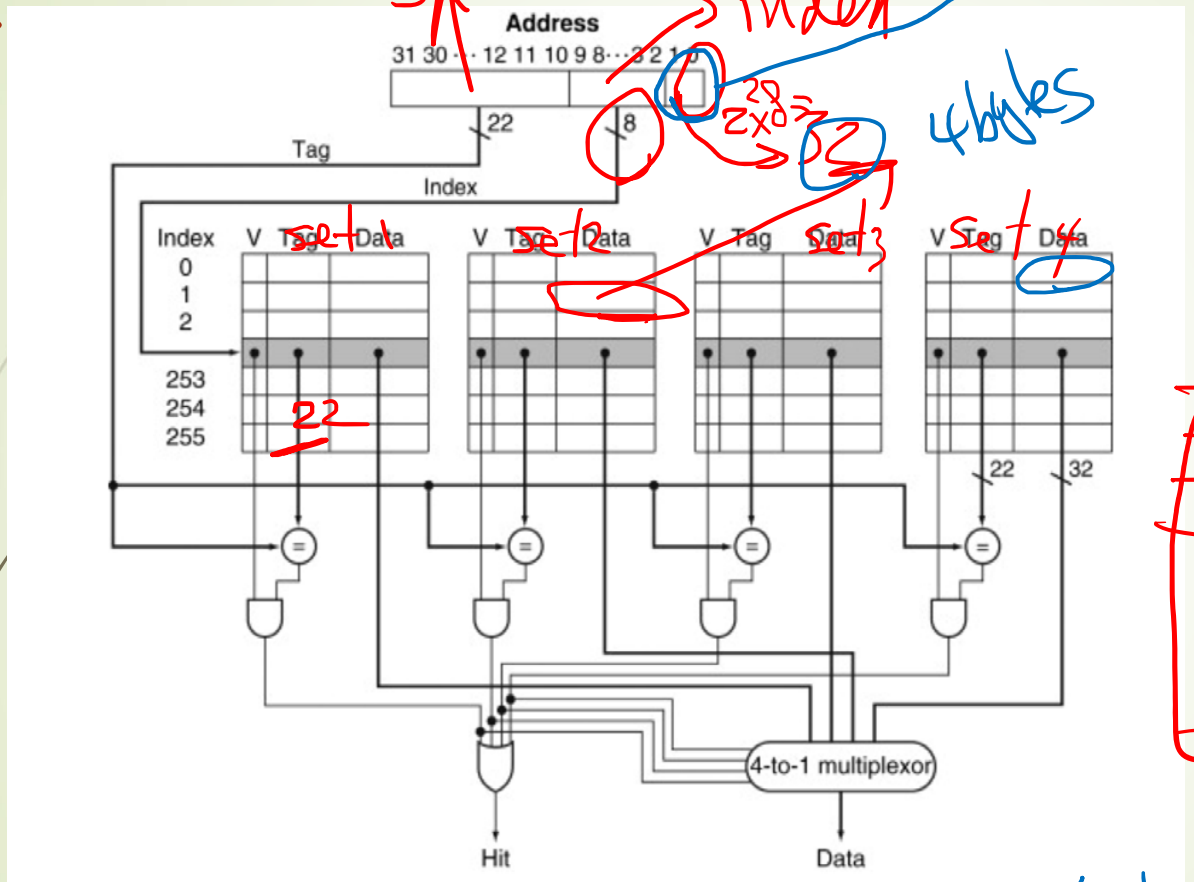
7,9,6,5,1,6
M M M M M H



7 Miss
9 Miss
6 Miss
5 Miss
1 ~~Hit~~ ~~Miss~~ Hit
6 Hit



3) What kind of cache memory is depicted below:



Tag

index

Byte offset

4 way associative

4bytes

$2^8 = 256$

256x4x4 → 4 bytes

0

1

2

255

4K Cache

4) The ____ of every cache block within the appropriate set of a set-associative cache is checked for a match against the memory block address.

- ○ index
- ◉ tag
- ○ block offset

Correct

The tags of all the blocks in the set must be searched to determine if the memory block is contained in the cache.

5) A four-way set-associative cache with 32-one word blocks requires ____ comparators to compare the tags of each element within the set.

- ◉ 4
- ○ 8
- ○ 32

Correct

4 indicates the numbers of blocks within a set and the number of comparators to determine which element of the selected set matches the tag.

6) A direct mapped cache with 32-one word blocks requires ____ comparator(s) to compare the tags of of an element with the memory block address.

- ◉ 1
- ○ 32

Correct

A single comparator is needed because the entry can be in only one block of the cache.

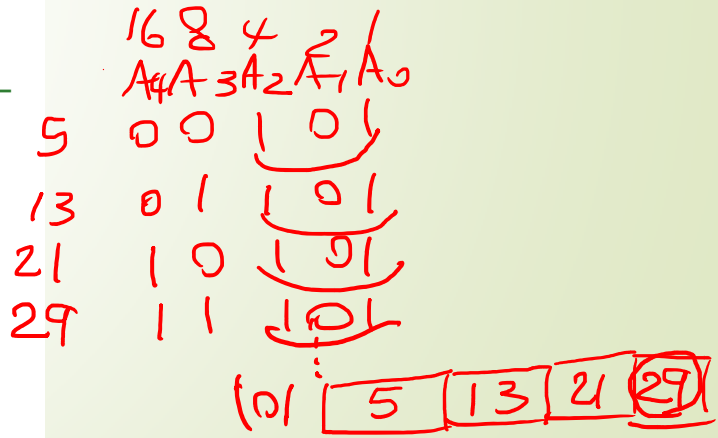
7) Which block in the cache is replaced by memory block 29?

Cache configuration: 4-way set-associative cache with 8-one word blocks
Replacement scheme: LRU
Sequence of previously accessed block addresses: 5, 13, 21, 13, 5
(Note: All memory block addresses map to cache set 1)

- ○ Mem[5]
- ○ Mem[13]
- ○ Mem[21]
- ◉ None. An element in set 1 is unused, so Mem[29] is placed in the fourth element of set 1.

Correct

The cache has two sets (0 and 1) and 4 blocks per set. The fourth block of set 1 is unoccupied, thus Mem[29] is placed in the fourth block of set 1. The replacement scheme has not yet been used.



8) Design a two ways set associative cache with the following parameters:

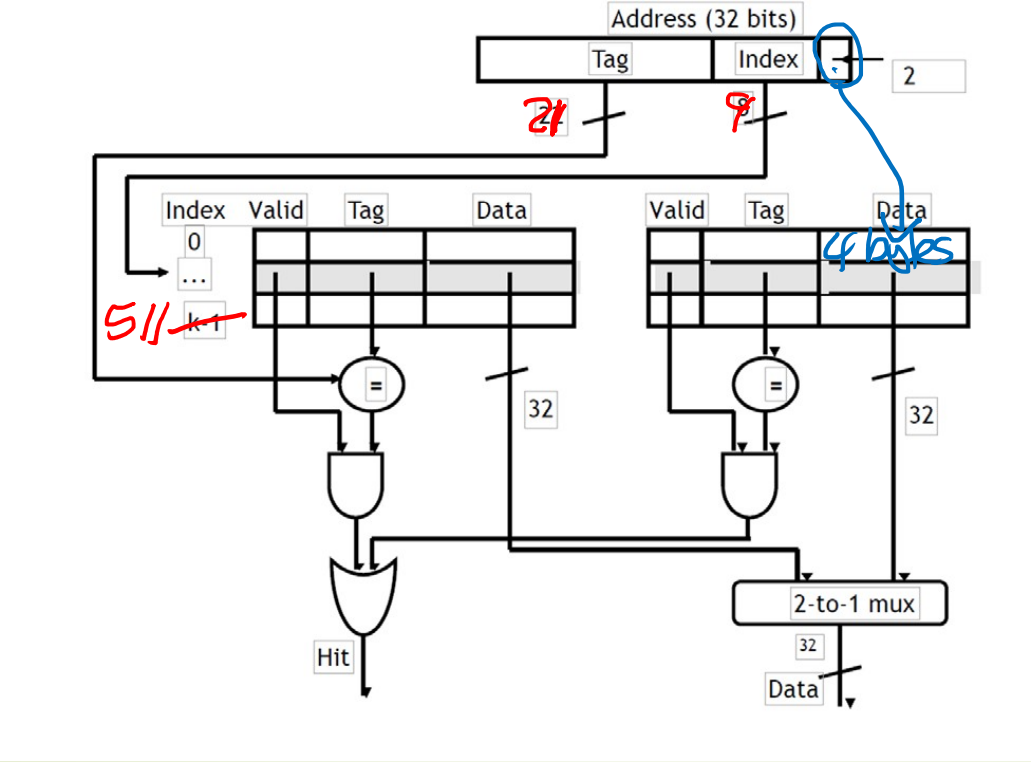
- Address size: 32 bits
- Cache data size: 4 KB
- ~~Cache block~~: 1 word (4 bytes)

word size

4k ÷ 2 = 2 k each

2k ÷ 4 = 512 words

2^9



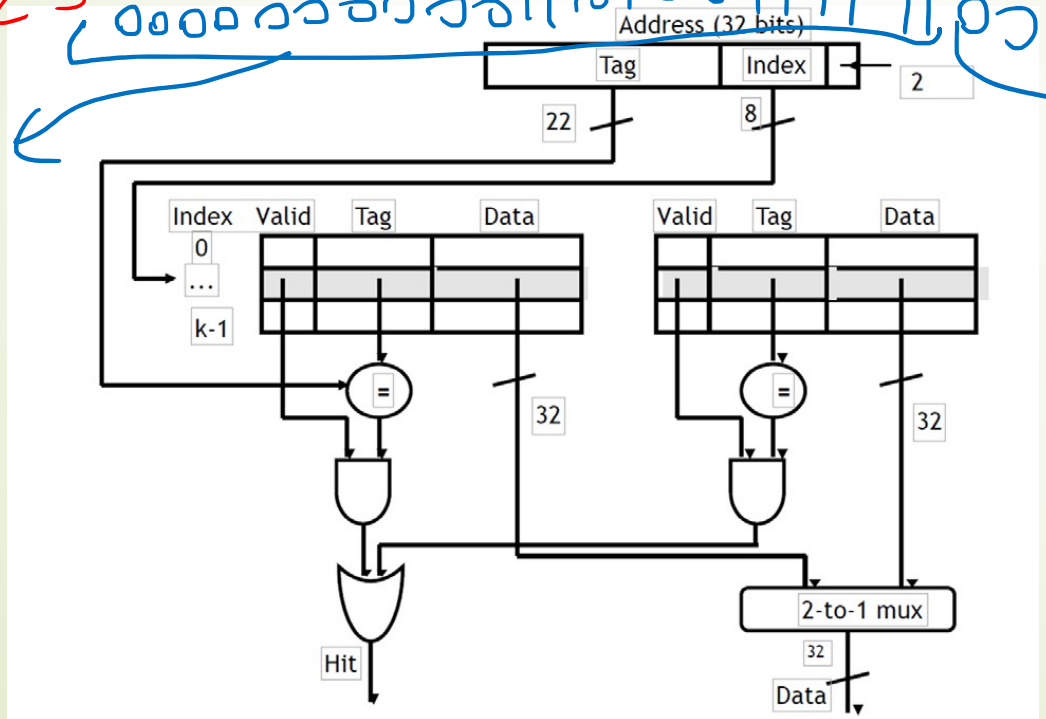
32 − 11 = 21

tag

9) For the following depicted diagram

a. Identify the cache architecture → 2 way Associate
b. What is the total cache size in words?
c. What is the index and tag when accessing memory location 0x0034FC08?

$2^8 = 256 \times 2 = 512$ words $* 4 = 2$ kB



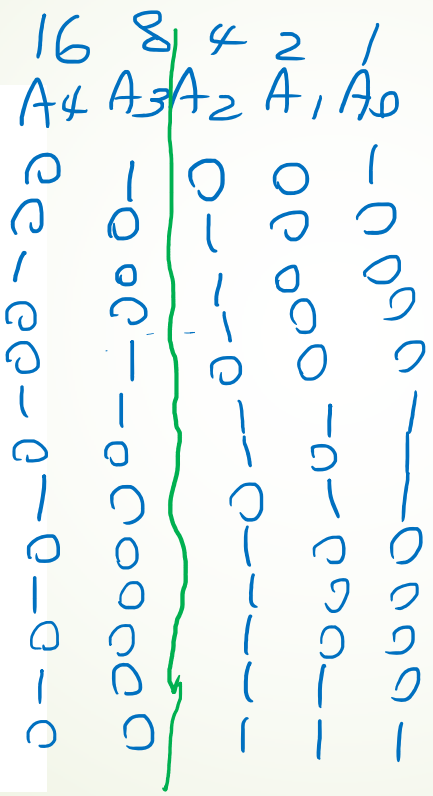
tag

index → 2

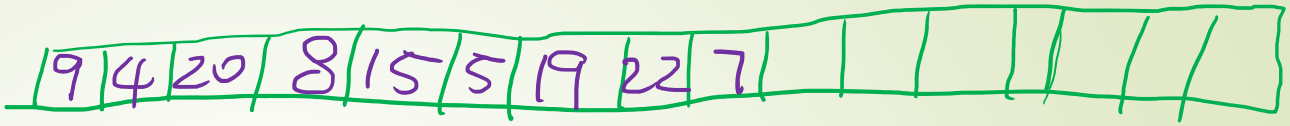
10) The following is a series of address references given as word addresses: 9, 4, 20, 4, 8, 15, 5, 19, 4, 20, 4, 22, 7, 17, 10. Assume a cache with a capacity of 16 words and the word size of 1 byte → No byte offset

a. For two ways set associative, show the hits and misses and final cache contents. Location

Location	Hit/Miss?
9	M
4	M
20	M
4	H
8	M
15	M
5	M
19	M
4	H
20	H
4	H
22	M
7	M



b. For a fully associated cache, show the hits and misses and the final cache contents.



Location	Hit/Miss?
9	M
4	M
20	M
4	H
8	M
15	M
5	M
19	M
4	H
20	H
4	H
22	M
7	M

11. Assume an instruction cache miss rate for an application is 2% and the data cache miss rate of 4%. Assume further that our CPU is running at 2 GHz and has a CPI of 2 without any memory stalls. The main memory access time is 100 ns.

a. Determine the overall CPI with the indicated misses, provided the frequency of all loads and stores in the application is 20%.

b. Suppose we like to add a second level cache with an access time of 5 ns, which has an instruction miss rate of .5% and data cache miss rate of .8%. Determine the overall CPI.

2GH → .5ns

100ns => 200 cycles

a. CPI = 2 + 2% * 200 + 4% * 20% * 200 (2% per instr.)

= 2 + 4 + 1.6 = 7.6

b. CPI = 2 + 2% * 10 + 4% * 20% * 10 +

.5% * 200 + .8% * 20% * 200

= 2 + .2 + .08 +

= 3.6